

A review on high speed and low power CMOS optical interconnects

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ABSTRACT- To satisfy the demand for inter chip interconnects bandwidth, current research projects are based on use of wave guided optical interconnects. The circuit is implemented to compensate high external capacitive loads. A maximum of 12 channels LASER diode each 10 GB/s is designed to reduce power consumption. The layout area, adjustable modulation current and bias current are achieved. Design can be used in high speed optical chips. The VCSEL's and power diodes are also used to provide optimized high speed and performance of optoelectronic devices. For high speed, photonic ring modulator is designed at 25 GB/s. In these VCSEL drivers i.e. common source (CS), CS with source degradation and source follower is presented. Various CAD tools are used for implementation of CMOS based optical circuits. This paper is a review of design of different VCSEL's and LASER driver circuits which are implemented on 180nm, 90nm and 65nm CMOS technology. The performance of various circuits is evaluated and compared in terms of power, power consumption, speed and maximal eye opening etc.

Keywords-Optical Interconnects, Vertical Cavity Surface Emitting Laser, Photo Detectors

1. INTRODUCTION

In deep sub micrometer VLSI technology for gigabit high speed communications optical interconnects are advantageous than electrical interconnects [1]-[6]. In Optics crosstalk, wave reflection, impedance matching, voltage isolation, and pin inductance are the major problems. As we know due to the scaling effects, interconnection problems and large-bandwidth optical interconnects are good solutions. Many new techniques exist that can also solve the problem of cost and helps to achieve economy [7]-[17]. A dense high speed, low power CMOS optical interconnect architecture is used. VCSEL data rate can be increased for given average current and reliability level. With the scaling of data rates, equalization circuits are used to compensate for frequency dependent loss of band limited channels. A good solution to this I/O bandwidth problem is the use of optical interchip communication links. I/O technology for high speed CMOS transceiver as shown in fig. 1.

This paper shows a brief review of the literature published during 2001-2015 based on silicon photonics. There view is a fast starting of various journal, articles and conference proceedings. The complete paper shows clearly that the new scientific technologies continue to be pushed and that the technology is developing faster.

Results in the form of table are presented and discussed at the end of the paper.

Comparison between optical interconnects and electronic chips have been the matter of research for the last 20 years [17]. Implementation of optical interconnects to chips would also face many technical problems. If we want superficially to impact interconnections on-chip or chip-to-chip, we need to consider technologies that can allow close packed optical interconnects at the chip level, by which we mean at least thousands or more of optical interconnects for each chip.

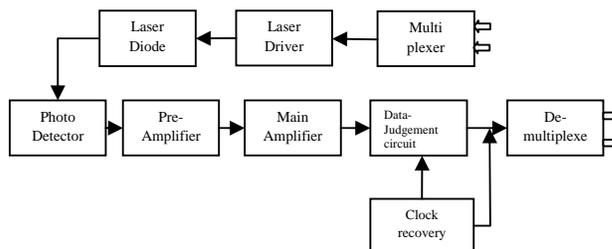


Figure 1: Optical I/O Technology [13]

A major research is for the development of Germanium (Ge) lasers. The advantage of Ge in silicon-based LASERS continues to increase. Germanium forms the active region for fabrication of photo detectors, electro optical modulators and recently the lasers. The main motive is electrical injection of doped tensile Ge to create a laser. Ge-on-Si has buildup its position as the preferred photodiode for CMOS photonics. Various design techniques using laser for ultra- high speed VCSEL circuit in CMOS process is made. Design technique for ultra-high speed VCSEL driver in 65 nm CMOS process is designed to verify the effectiveness. In the last years, optical interconnects have commonly used for high speed applications. These optical modules provide greater interconnect bandwidth by supporting longer links, high data rate and low power consumption than electrical links.

II. LITERATURE REVIEW

In 2001 using TSMC 0.18 μm CMOS 1P6M technology, authors developed an optoelectronic

transceiver that can operate at 2.5 Gb/s for optical communication [1]. To get high speed operation the proposed optical transceiver senses the photo current and generates O/P voltage. The laser diode driver with programmable driving elements is designed. The proposed transceiver is used for low cost low power chip to chip interconnection and fiber communication system. A low cost and low power transceiver is designed by 0.18 μ m CMOS technology. The transceiver consists of photo detector and transmitter with laser diode driver and VCSEL laser diode. This proposed optical transceiver can be widely used in various chip to chip interconnections and fiber-optic communications at low cost and low power. The various results shows that the maximum power consumption is 0.167 mW for TSMC 0.18 μ m CMOS. A 30 Gb/s parallel optic-fiber receiver is also used. This design has been implemented using TSMC 0.25 μ m CMOS technology [2]. For low power and high density links, fast VCSEL drivers were designed for 90 nm SOI CMOS [3]. The three VCSEL drivers i.e. common source, common source with source degradation and source follower is presented. The supply voltage is 1V. Comparison between power optimized topologies is implemented on 90 nm CMOS technology. These drivers were optimized for maximal eye opening. These VCSELs driver with a bandwidth of 18 GHz give the lowest power consumption [3].

A new design technique is used for CMOS based optical transceiver capable of 240 Gb/s bidirectional data rates. In this technique a CMOS chip having 16 Tx and 16 Rx channels are used. All Tx and Rx channels operate at a speed up to 15 Gb/s for an aggregate data rate of 240 Gb/s. The area efficiency of 14 Gb/s/mm² per link is the highest efficiency [4]. The circuit schematic of complete receiver amplifier using Trans Impedance Amplifier (TIA) and Limiting Amplifier (LA) is designed. VCSEL and PD arrays were designed at 985nm technology. The transmitter was powered with a 1.8 V supply for pre drivers and 2.7 V for output stage. The rise and fall times and RMS jitter extracted from 10 Gb/s is calculated from eye diagram. The effect of fall time compensation technique was considered by measuring sensitivity and timing margin for transmitter. Inter channel receiver crosstalk was investigated at the opto chip level through sensitivity.

To assess the impact of channel to channel crosstalk, the original measurements were compared to the other channels when different combinations of channels were using optical data. Crosstalk testing identified a constant pattern of power and timing margin based on location of channel within receiver block. At the receiver side 1.8 V to core and buffer supplies provide a tradeoff between performance and power dissipation. Above techniques shows that CMOS based optical transceiver that supports aggregate bidirectional data rates up to 240 Gb/s for 16 transmitter and 16 receiver channels can be designed. Thus the total power consumption for receiver and transmitter is 2.15 W [4].

All 16 transmitter channels exhibited open eye at 20 Gb/s data rate. A low power 16 \times 10 Gb/s bi-directional CMOS optical transceiver is designed with 0.13 μ m technology. 16 channel photodiodes and VCSEL arrays provide optical interfaces to the chip. This work shows that at 985 nm opto chips gives better area efficiency [5]. Opto chips using the features of 985 nm transceivers give high performance CMOS analog amplifier circuits. Waveguides at 850 nm gives lower optical loss. These transceivers use optical data buses for interconnect distance up to 1m.

To remove the problems of low power in CMOS chips a design technique of a 40 Gb/s VCSEL driver using analog communication technique in 90-nm CMOS is used in 2010. In this paper a circuit is designed having two emphasis circuits for both negative and positive edges of clock is designed to implement asymmetric emphasis technique at 90nm CMOS for optical interconnections. The eye at a rate of 10 Gb/s using 90nm is generated. The FIR filter used at the output of the VCSEL counterbalance for the loss due to parasitic elements by generating emphasis in high frequency region [6]. This helps to improve the waveform generated for current flowing through VCSEL and results in good eye open. The pre-emphasis technique used in VCSEL driver is shown in Fig. 2.

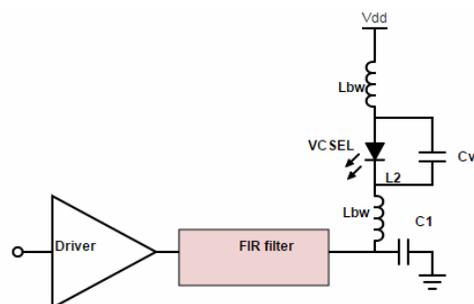


Figure 2: Emphasis technique used in VCSEL [6]

In 2010 an IBM research Centre proposed a fabrication technique for board level interconnects. In this technique 24 channel bidirectional optical transceiver module based on TSV Si carrier for board level interconnects is made. In this paper IC's and Opto Electronics (OE) are designed for 10 Gb/s and 15 Gb/s operation with bi-directional aggregate bandwidths of 240 to 360 Gb/s for 48 channels [7]. In this opto chips are assembled to increase the speed and high density to form full optical modules has been developed and demonstrated. Firstly the electrical connections between through silicon vias carrier and CMOS IC's have been verified by measuring I/O impedance of 24 Tx and 24 Rx channels. In receiver, connection between IC and Photo Diodes (PD) chips were estimated through biasing each of 24 photodiodes. High speed can be characterized by modules at data rates up to 20 Gb/s. pseudo random bit sequence (PRBS) pattern of length

2^{7-1} have been generated to the form of eye diagram. VCSEL and PD arrays have been fabricated and characterized by dc electrical measurements. A flip-chip bonding technique was developed to form 850nm optically enabled multichip module. The electrical characterization of complete module at high speed shows receiver channels operating up to 12 Gb/s and Tx channels up to 15 Gb/s.

To decrease the ringing phenomenon at both edges of clock different compensation techniques are used. The dependence of eye opening height and jitter at 10 Gb/s on Extinction Ratio (ER) using any emphasis technique is calculated. Conventional symmetric technique can counterbalance for influence of parasitic effects but these cannot reduce nonlinear effects of VCSEL. To solve this problem asymmetric emphasis technique is proposed. This helps to enable and control the delay, width and height of emphasis pulse at both the edges. To overcome the problems of data rate and sensitivity a 25 Gb/s monolithic optical transmitter with micro-ring modulator in 130-nm SoI CMOS is designed in 2013 [8]. In this paper high speed photonic ring modulator is designed at 25 Gb/s. It is measured at bit error rate of 10^{-12} . Power consumption is 17 mW with energy efficiency of 680fj/b. 130nm CMOS SOI process has been demonstrated for 25 Gb/s using MZM or pre-emphasis techniques with Si rings to compensate bandwidth limitations. Simulations at 25 Gb/s and 15 Gb/s were carried out. The bit error rate from eye opening diagram with +1.2 V /-1.2 V power supply for different data rates can be measured. This has been demonstrated that it gives highest performance at lowest energy efficiency using optical transmitter. It removes the need for pre-emphasis circuit for 25 Gb/s. This work can be demonstrated at 45nm with low power. This transmitter is not capable of achieving power as low as that of using advanced digital process. In 2013 a CMOS IC design based on fabrication and characterization of 48 channel optical transceiver is made for terabit/sec data transfer rate. A dense holey CMOS chip using 24 VCSEL's and 24 power diode arrays is designed [9]. The optimized results at 850 nm VCSEL/PD's provide high speed by integrating optoelectronic devices. High speed measurements using transmitter and receiver are carried out. A transmitter and receiver channel at 15 Gb/s and 20 Gb/s under same running conditions are used. The transmitter at different supply voltages were carried out for pre-driver stage and for Output driver stage. Similarly 24 receiver channels at 20 Gb/s and 15 Gb/s were used. High speed data using receiver power supply at 1.9 V was obtained. The single channel power consumption is in range of 75-80 mW. One useful parameter sensitivity can also be measured by considering eye at 10 Gb/s, 15 Gb/s and 22 Gb/s. The average sensitivity for 12 channels at BER of 10^{-12} at 15 Gb/s is nearly -10dBm. Sensitivity for 24 channel transmitter and receiver opto module at 20 Gb/s can be estimated from eye diagrams. The opto module at high speed can provide an efficiency of 7.3 pJ/bit for

both transmitter and receiver [9]. As the wavelength is well established standard, the attainment of VCSEL based link operating at 850 nm is powerful but energy efficiency of the system is better if wavelength is increased to allow more design mould ability. The optical link with a 1060 nm wavelength controlled by low power CMOS IC at 20 Gb/s gives total efficiency lower than 5pj/bit. Power dissipation in VCSEL circuit is less than transmitter total power consumption [10]. Finally VCSEL and photodiode using wavelengths in the domain 860-1160 nm can be implemented to realize high bandwidth.

With the progress in information and communication technology, high speed i.e. 25 Gb/s, low power and short reach communication that achieves high throughput is becoming more important and will continue to increase. To obtain high speed a design technique for CMOS optical transceiver using analog front end and data format conversion is used in year 2014 [11]. With the degradation of optical link due to power supply variations, a noise tolerant 25-Gb/s analog FE is proposed, with a fully differential laser diode driver. The transmission performance of transceiver at 25 Gb/s and 6.25 Gb/s can be confirmed by eye diagrams. At full channel operation the total power consumption measured is 2.2 W. A trans impedance amplifier using laser driver with 4×25 Gb/s with 2.2 W power consumption at 65 nm CMOS technology is designed [11]. The eye diagram of TIA at 25 Gb/s operation shows low peak to peak jitter and eye amplitude. To calculate the speed and power dissipation a high speed, radiation tolerant laser drivers in 0.13 μ m CMOS technology has been implemented in 2014. In this pre-emphasis circuit is implemented to compensate high external capacitive loads. It has been designed using 0.13 μ m technology at 2.5V. The power consumption of gigabit laser driver is 8.9mW and 55mW for low power giga bit laser driver [12]. VCSEL and edge emitting laser diode can be used as laser diode but the power consumption of diodes is very high especially VCSEL. Extra wastage of power is serious problem when used as an optical links. Therefore a low power driver has to be implemented called low power GBLD at 5Gb/s using VCSEL diodes. Both GBLD and LpGBLD have been designed and implemented with 0.13 μ m technology. The GBLD gives high performance at rate of 10 Gb/s. LpGBLD gives performance at rate of 5 Gb/s. Power consumption of LpGBLD is 38% lower than that of GBLD [12].

A new technique for design of 12 channel 120 Gb/s laser diode driver in 0.18 μ m CMOS technology is designed for high speed optical chips. In this 12 channel LASER diode each with a 10 Gb/s at a power consumption of 98mW is designed in 0.18 μ m technology. The supply voltage is .18 V. The layout area, adjustable modulation current and bias current are achieved. This design can be used in high speed optical chips. In this high performance laser is designed for

optical interconnection. It operates at 98mW power dissipation and 10 Gb/s×12 data rates. In an optical transceiver, a laser diode driver plays a major role, which converts digital signal to large voltage or current signal, to drive external laser diode as shown in Fig. 3. One channel laser diode driver consists of three stages, the input stage, pre-amplify unit and output stage.

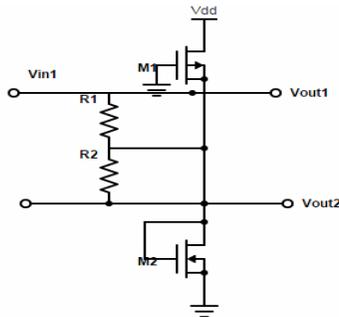


Figure 3: Input stage, pre-amplifier unit and output stage circuit [13]

The one channel laser driver circuit for 10Gb/s with voltage from 1.4V to 1.8V gives power dissipation of one channel driver circuit is about 98mW with 8.7 GHz bandwidth [13]. The driver circuit can generate adjustable modulation current from 1mA to 16mA and bias current from 1mA to 10mA. Hence the 12 channel laser diode driver array can be used in high speed optical chips. In the year 2014, 22 Gb/s VCSEL driver circuit in 65nm CMOS process is made. A compensation technique for ultra- high speed VCSEL based on pre-emphasis is used to model output current waveform. For gigabit high speed communications optical interconnects are advantageous than the electrical interconnect. Below Fig. 4 shows a VCSEL driver load model.

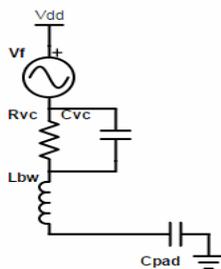


Figure 4: VCSEL driver load model [14]

Lbw is the bond wire inductance, Rvc is equivalent resistance of VCSEL, Cpad is the total parasitic capacitance in output node. Digital pre-emphasis can be done by reversing, delay, changing amplitude and

adding the adjusting signal to the original one. Delay time is generally very short; mainly to speed up the jumping edge but bond wire inductance has already used to speed up the jumping edge. So in this paper compensation technique is used to reduce the inter symbol interference caused by ringing. Inter symbol interference can be verified by comparing the quality of output current eye diagram before and after compensation technique. This compensation technique reduced the jitter of eye diagram from 8.5ps to 2.5ps [14]. With the decrease in jitter, speed and power dissipation is also calculated. To improve the bit error ratio NRZ modulated 850 nm VCSEL is designed for increased data rate ie. 50Gb/s up to 90 degree Celsius [15]. The demonstration of high temperature operation at 50 Gb/s is necessary. 850 nm VCSEL transmitter operating at 30 to 90 degree Celsius with driver shows the transmit equalization. This is characterized in terms of BER and jitter. The maximum operating temperature is limited to 57 degree Celsius. Next the performance is calculated from 25 to 28 Gb/s devices in terms of the bias current densities used for experimental results.

Optical interconnects are major task in technical field and a golden chance for high data applications. Now days a very fast, efficient optical communication links are going to make on chip, board-to-board, chip-to-chip interconnects.

The main important task is intra-chip optical communication. Most of the research laboratories are working on intra chip optical communications for various processor cores on a chip. To use these required optical paths that are scale able to thousands of cores, new wavelength-multiplexed architectures must be devised using WDM and DWDM approach. These communication techniques are used to calculate the maximum data rate achieved. WDM multiplexes a number of optical carrier signals on to a single optical fiber by using different wavelengths of laser light. DWDM has a capability to transmit up to 80 channels wavelengths with all wavelengths in 1550nm region. DWDM has advantage to amplify optical channels. Another approach to view the future photonic CPU is the macro chip in which four dies are bonded to a common silicon on insulator substrate along with DRAMs. These macro chips provide electrical and optical communication between the chips by using a network of silicon waveguides [17]. The intra chip optical communication, which uses the hybrid-integrated GaAs light sources, is also moving along well to create active region [6]. For 2-3 Gb/s board-to-board optical interconnects, the silicon optical insulator plays a significant role.

RESULTS AND DISCUSSIONS

A summary of the results and their comparative analysis is tabulated in the Table 1. In this table NA means that parameter is not available.

Table 1. Summary of results in tabulated form

Speed Gb/s	Technology	Wavelength nm	Area	Jitter	Vdd	BER	OMA	Power consumption	Reference
12.5	0.9μm	NA	NA	NA	1 V	<10 ⁻¹²	2.6dBm	72.7m W	[3]
20-TX	NA	985nm	14	NA	NA	<10 ⁻¹²	1	73	[4]
12.5-RX	NA	985nm	14	NA	NA	<10 ⁻¹²	-8.5	62	[4]
12.5-TX FOR HS	0.13μm	NA	NA	1.8ps	1.8	<10 ⁻¹²	>1	73	[5]
10 TX FOR LP	0.13	NA	14	2.7	1.45	<10 ⁻¹²	-1.5	39.5	[5]
12.5 RX FOR HS	0.13	NA	14	2.7	1.8	<10 ⁻¹²	-11.5	62	[5]
8 RX FOR LP	0.13	NA	14	5.6	1.1	<10 ⁻¹²	-8.3	17	[5]
10	90 nm	NA	NA	6	NA	<10 ⁻¹²	NA	50	[6]
15 –TX	NA	850nm	NA	OPEN EYE	2.1	<10 ⁻¹²	NA	NA	[7]
12.5-RX	NA	850nm	NA	OPEN EYE	2.2	<10 ⁻¹²	NA	NA	[7]
25	130nm	NA	NA		2.4	<10 ⁻¹²	NA	17	[8]
12.5	90nm	850nm	31.8	OPEN EYE	1.9	<10 ⁻¹²	NA	3W	[9]
15-TX	NA	850nm	NA	OPEN EYE=0.8	NA	<10 ⁻¹²	NA	27.4	[10]
20-RX	NA	1160nm	NA	OPEN EYE=0.8	NA	<10 ⁻¹²	NA	70.9	[10]
25	65nm	NA	3.6×5.4	18.4	2.5	<10 ⁻¹²	-6	2.2W	[11]
5 FOR TX	0.13μm	NA	4×4	27	2.5	<10 ⁻¹²	NA	29	[12]
5 FOR RX	0.13μm	NA	4×4	0.9	2.5	<10 ⁻¹²	NA	55	[12]
10	0.18	NA	0.13	<5ps	1.8	<10 ⁻¹²	NA	98	[13]
50	130nm	850nm	0.11	1.3ps	NA	<10 ⁻¹²	-8.5	1.775W	[15]

The laser drivers were used for the implementation of optical data communication using different technology nodes. The CMOS laser drivers designed above were implemented to increase speed and decrease power consumption. Above review shows the comparison between different laser drivers. Researchers mainly emphasized to design both the laser device and laser driver. In all the papers simulations were carried out for transmitter and receiver with same bit error rate. The performance of these circuits was measured in terms of bit error rate and opening and closing of eye. The co-design approach used for implementation of low power and high speed optical transmitters and receivers can be used for optical data communication. As seen from the above table power consumption also varies with technology. At the side use of low power and high speed laser driver, bandwidth enhancement is also the

factor of concern that was also used to design laser driver for high modulation current.

CONCLUSION

All the silicon based CMOS laser drivers were designed by using different topology to minimize undesirable noise. The laser driver was implemented using mixed signal CMOS technology through MOSIS foundry using different technologies and having minimum feature size. The performance of all the designed laser driver has been verified with bit error rate measurement, power dissipation, OMA and eye opening height at different data rate like 12 Gb/s, 10 Gb/s non return to zero pseudorandom bit pattern. To reduce the effect of parasitics decoupling techniques are used and capable of producing intended results from.

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