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An Ultra Low-Voltage CMOS Self-Biased OTA

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***Abstract*— An OTA (Operational Transconductance Amplifier) is designed for low voltage and low power operations. Differential amplifier is the most important amplifier in the analog design circuits because of its good performance as input amplifier. In this paper, the three stage OTA is designed using 65nm CMOS technology. The input stage of the OTA is designed using the bulk driven MOS pseudo differential pair, provide rail-to-rail output range with the minimum supply voltage. The characteristics of OTA giving in terms of common-mode, power supply rejection ratio, voltage gain and power consumption. The self biasing technique is used to bias the OTA which in turn enhances the performance of OTA and eliminating the need of extra biasing circuitry. The measured output for the OTA provides the dc gain of 46 dB for the supply voltage 0.5 V. At voltage 0.5 V the measured power dissipation is 124µW.**

Keywords- OTA, CMRR, PSRR, Ultra-low-voltage.

I. INTRODUCTION

From last few years the integrated circuit design is gone towards the low voltage and low power supply techniques as in the increasing demand for portable systems. Low voltage power supply technique has more importance in the portable applications. Low voltage analog circuit designs are greatly different from large voltage analog circuit design. So there is need for some design techniques to match the low voltage design. The current mode approaches are good alternative method for low voltage with high performance analog circuit. Current levels are more concerned in current mode methods for the operation of circuit.

Also the small channel-length CMOS transistors operate by the low voltage power supply. The supply voltage for low power applications is set for less than 0.5V in coming years. But this continuous reduction in the supply voltage and channel-length of transistor has destroyed the performance of analog circuitry. Probably, it affects the device intrinsic gain, output voltage swing and common mode range. In order to increase the gain of OTA multi-cascading techniques are more preferable over the conventional cascading techniques and also the technique is often used for low voltage operations. Also, to improve the range at output and input of amplifier, various design techniques were introduced for example level-shifting, self-cascading, floating gate transistor and bulk biasing. For various systems and for analog circuits an OTA used as important building blocks. Depending on circuitry, an OTA satisfy many design requirements. Working principle of conventional OTA is based on VCCS (Voltage Controlled Current Source) i.e. it produces output current for input voltage.

This paper proposed an OTA design operated at sub-1V power supply as well as achieving rail to rail input range at the output of the amplifier. Bulk-driven MOS transistor and pseudo- differential amplifier technique are used to obtain rail to rail input range with ultra low voltage power supply. And to improve the performance of the OTA a novel biasing technique is introduced which in turn, eliminates the need for extra biasing circuitry. These proposed methods enhance the power-supply rejection ratio and common-mode rejection of the OTA.

Now, in section II, discuss the techniques and input-stage design used to obtain rail to rail input range and low supply voltage operation. In section III, proposed biasing technique is describe. Section IV, frequency compensation scheme set up in the OTA. Circuit design of the OTA is then discuss in the section V while section VI gives the conclusion of the paper.

II. DESIGN OF INPUT-STAGE AND TECHNIQUES FOLLOWED

The OTA technique to obtain rail to rail input range, complementary differential pair is used show in Fig. 1. To provide adequate amount of transconductance one of the two complementary differential pair should be fully on over the range of 0 to $V_{DD\,min}$. For low common mode input, the NMOS differential pair is off and PMOS differential pair is operates in saturation. For high common mode input, the PMOS differential pair is off and NMOS differential pair operates in saturation. As a result, it provides the rail to rail common mode because complementary differential pair is always working. Here, it is important to note that the input level in the middle region of the supply, both the differential pairs is on which elevates the transconductance level. Using the architecture the supply voltage given by the expression $V_{DD\,min} = V_{GS\,n} + |V_{GS\,p}| + 2|V_{D\,sat}|$[1]. If the supply voltage is less than $V_{DD\,min}$, both differential pair are turned off at the same time for the input common mode values besides the middle of the supply range.[4][5].

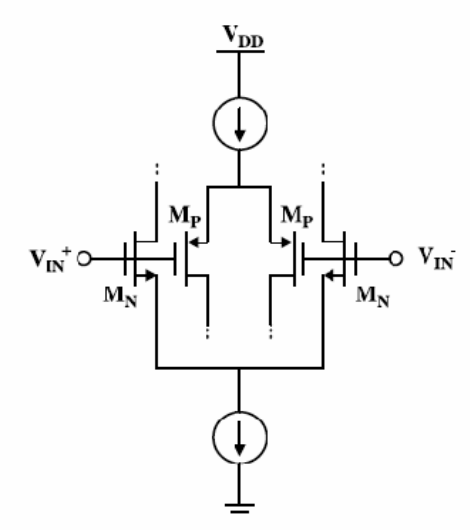


Fig. 1 Complementary differential pair[1]

A. Bulk-Driven MOS Transistor

Bulk-driven MOS transistor [6] technique commonly use for low voltage analog circuit. The operation principle of the bulk-driven MOS is similar to the JFET. It is the good solution to overcome the threshold voltage. The operational principle of the bulk-driven method is that the gate-to-source voltage is set at the point which is enough to form an inversion layer and the input signal is also applied to the bulk terminal. In this way the threshold voltage is either eliminate or decrease in signal path. The circuit and the cross-section of bulk-driven transistor is shown in the Fig. 2. The bulk-driven transistor is function as depletion type device which operates with the zero, negative and slightly positive bias voltage. Thus, bulk-driven technique permits the smaller voltage to be applied at the input terminal. The bulk voltage affects the thickness of the inversion layer, the drain current can be adjusted by changing the bulk voltage via the body.

The major advantage of using bulk-driven transistor is the ON/OFF ratio of large voltage which is used for modulation. Although overcoming the threshold requirement there are the several disadvantage of bulk-driven transistor. First, the transitional frequency of the gate-driven transistor is greater than bulk-driven transistor which reduces the speed and bandwidth. Second, noise performance of the bulk-driven transistor is poor than the gate-driven transistor. Third, transconductance of the bulk-driven transistor is less than the gate-driven transistor.

B. Pseudo Differential Pair

The pseudo differential pair [8] with CMFF (common-mode feed forward) shown in Fig. 3(a). As shown in the figure it uses the separate transconductance for common-mode detection. This resulting topology increase load at the driving stage because of the connection of two input transistors, one for the common-mode transconductance and other for differential transconductance. As a result, it doubles the input capacitance. The PSRR (power supply rejection ratio) and CMRR (common-mode rejection ratio) of the circuit is then expressed as

$$\text{CMRR} = \text{PSRR} \approx \frac{1}{2} g_{m2} (r_{01} \,||\, r_{02}) \quad (1)$$

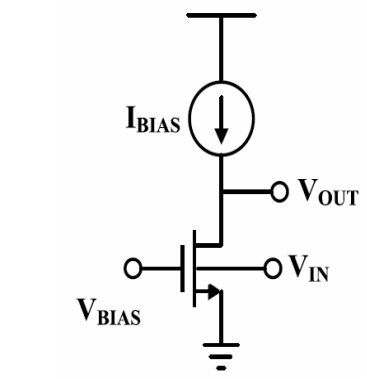


Fig. 2 Bulk-Driven transistor circuit[1]

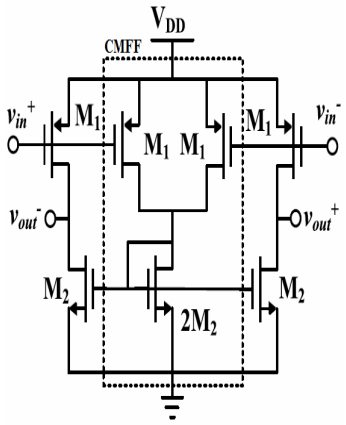


Fig. 3(a) Pseudo Differential Pair with CMFF[1]

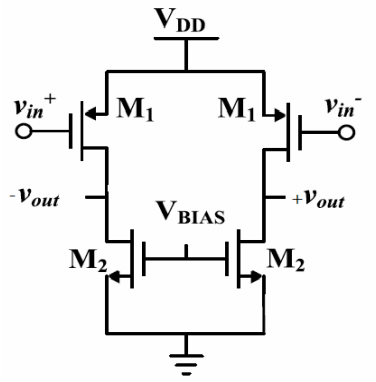
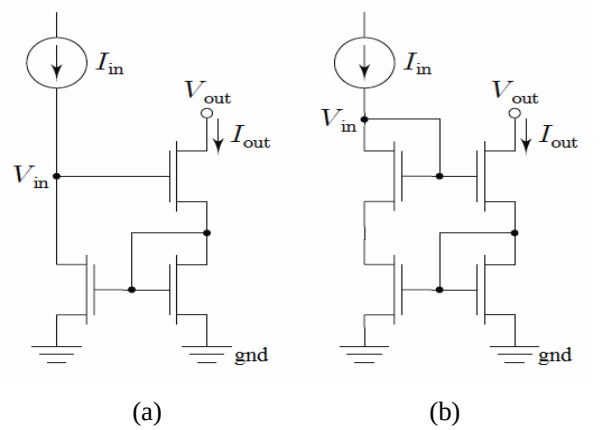


Fig. 3(b) Pseudo Differential Pair without CMFF[1]

The conventional differential pair without CMFF shown in Fig. 3(b) cannot be used. The disadvantage of using this type of

differential pair is the intense decline in the power supply rejection and the common-mode. To overcome this problem pseudo differential with CMFF is used here.



(a) (b)

Fig. 4 (a) The Wilson current mirror (b) The Super-Wilson current mirror[2].

C. Super Wilson Current Mirror

Current mirrors [3] are the major component in analog circuits. Current mirror is a circuit designed to reflect the current from one active device to another by controlling the current and holding the output current constant irrespective of loading. The simple current mirror is not suitable for low-supply-voltage design as it need input voltage of two (may be more, if deal with body effect) diode drops and saturation [2]. So, the Super-Wilson current [2] mirror taken into count as it functions at all levels from week inversion to strong inversion. The super Wilson current mirror is shown in the Fig. 4. The Wilson current mirror attains a high incremental output resistance. A diode connected transistor is used in the high swing Super-Wilson current mirror. It helps to reduce current mismatch between input current and output current by holding the drain of the mirroring transistor almost to the same voltage.

III. The Self- Biasing Technique

The three stages OTA with the proposed biasing technique [1] is shown in the Fig. 5. The first stage is the pseudo differential pair, second stage is common source stage with current mirror and third stage is common source stage with current source load. The designed OTA uses common-mode feed forward circuit of the first stage to bias the gate of transistor M_1 and M_5 in the second stage. Also, v_{out1} is used to bias the gate of the transistor M_8 in third stage which is shown by the dashed lines in Fig. 5. In this way, the OTA bias itself or in other words, there is no need of extra biasing circuitry to bias the OTA. The self-biasing technique reduces the power consumption up to 25% in comparison to that circuit which uses separate biasing circuit self-biasing technique also reduces overall area, supply noise and OTA sensitivity to common-mode voltage.

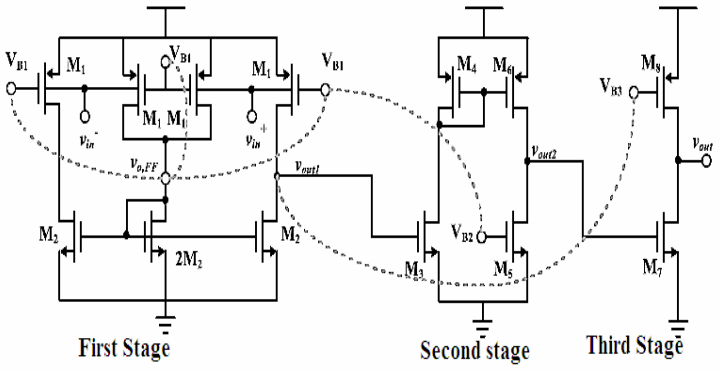


Fig. 5 Schematic of Self-Biasing[1]

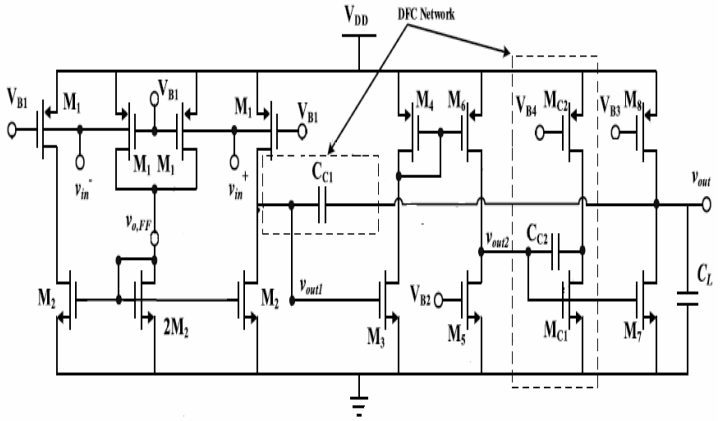


Fig. 6 Schematic for DFC network[1]

IV. Frequency Compensation

Frequency compensation network is used in the designed OTA. It is based on the DFC (damping factor control) compensation [7]. The proposed OTA with DFC compensation network is shown in Fig. 6. Frequency compensation is compulsory to stabilize closed-loop three-stage amplifier. The DFC network has two nested miller capacitors (C_{c1} and C_{c2}) in addition with DFC stage G_{mc}. The DFC compensation greatly intensifies the bandwidth in comparison to nested miller technique. To stabilize OTA, nested miller compensation uses two negative capacitive feedbacks as depicted where C_{c1} is for pole splitting and C_{c2} is for adjusting the damping factor of non-dominant poles.

Simulation of conventional nested miller technique and the DFC technique shows the improvement in the unity-gain frequency up to 3 times for the same phase margin and also for same power consumption and for the same driving load. Here, the value given to load capacitor is C_L = 3pF [1] and to miller capacitor is C_{c1} =550 fF and C_{c2} = 5pF [1]. It also enhances the large behavior of the OTA.

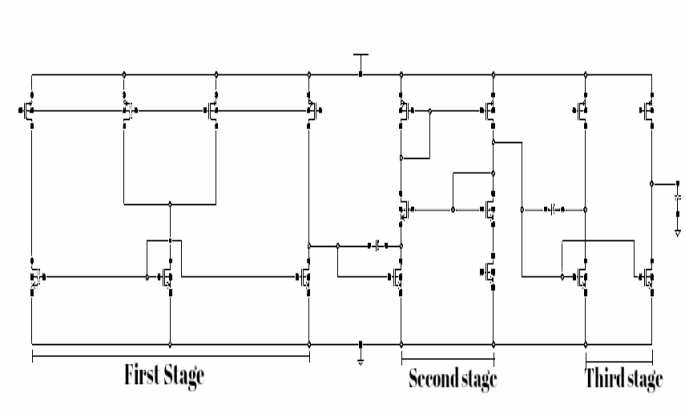


Fig.7 Schematic of proposed OTA

V. Proposed OTA Design

The schematic of the proposed OTA with frequency compensation, Super-Wilson current mirror and self-biasing is shown in Fig. 7. The proposed design consists of three amplifying stages. The first stage is the bulk driven pseudo-differential pair which had advantages of both (bulk-driving transistor and pseudo differential pair) technique depicted in the section II. The second stage is the common-source stage with Super-Wilson current mirror also described in section II. The third stage is the common-source stage with the current source. The first stage and the third stage are the inverting while the second stage is non-inverting. It is because, to sure the negative feed backs of the inner loops the third stage required to be inverted. So the second stage is load with super-Wilson current mirror and third stage is load with the current source.

In these three amplifying stages, the channel length of the transistor is set to 2 times minimum length to provide the enough intrinsic gain. To provide the current level, needed to attain the appropriate specifications width of the transistors is adjust. The voltage supply $V_{DD\,min}$ [1] is expressed by

$$V_{DD\,min} = |V_{GS1}| + V_{GS2} \quad (2)$$

So in case transistor works in sub-threshold region, means, $|V_{GS1}|$ $|V_{TH}|$ then $V_{DD\,min}$ can be less than the threshold voltage of PMOS and NMOS transistor. In this circuit, transistor's threshold voltage is set to 0.5 V for both PMOS and NMOS transistor.

VI. Results

The low voltage self-biased OTA was fabricated at 65nm CMOS technology. The OTA is designed to exploit the gain of 46 dB and the unity-gain frequency of 97 MHz at V_{DD} = 0.5 V. The phase margin is 52˚. The total dc power consumed by the OTA is 124 µW for V_{DD} = 0.5 V. The open loop-frequency response is shown in fig. 8. Fig. 9 represents the input and output waveforms of OTA at V_{DD} = 0.5 V. The measured slew rate is 77.2 V/µs for V_{DD} = 0.5 V and the waveform shown in fig. 10. The low frequency CMRR is measured to be greater than 30 dB while the PSRR is greater than 40 dB for V_{DD} = 0.5 V. Table I shows the performance parameters for supply voltage 0.5 V of OTA.

VII. Conclusion

The low voltage OTA is proposed for the low-voltage operation in CMOS technologies. The first stage or the input stage of OTA utilizes two low-voltage techniques i.e. pseudo-differential pair and bulk-driving MOS. The benefit of using these two technologies is that it provides the rail-to-rail common-mode operation and minimum supply voltage operation simultaneously. At second stage, Super-Wilson current mirror is used at does not have channel length modulation and increased output impedance which helps in increasing the gain and reduce power consumption. The OTA also deploys the self-biasing technique that eliminates the extra biasing circuitry and enhances the performance of OTA by reducing area and power.

The three stage OTA was designed on 65nm CMOS technology. The proposed OTA produces the gain of 46 dB for supply voltage of 0.5 V. The power consumed by the OTA is 124 µW. The CMRR of the OTA is 32.46 dB for V_{DD} = 0.5 V and PSRR is 53 dB for V_{DD} = 0.5 V.

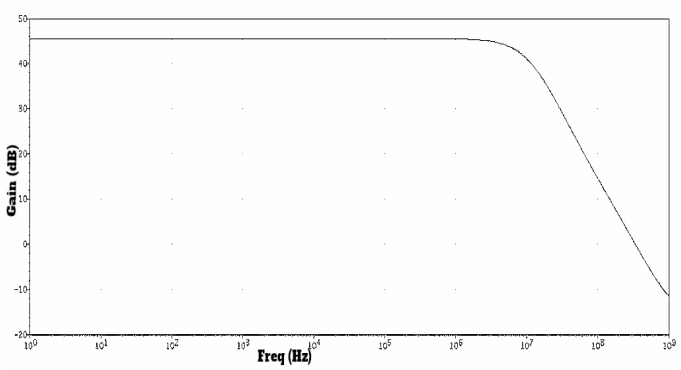


Fig. 8 Open Loop Frequency Response

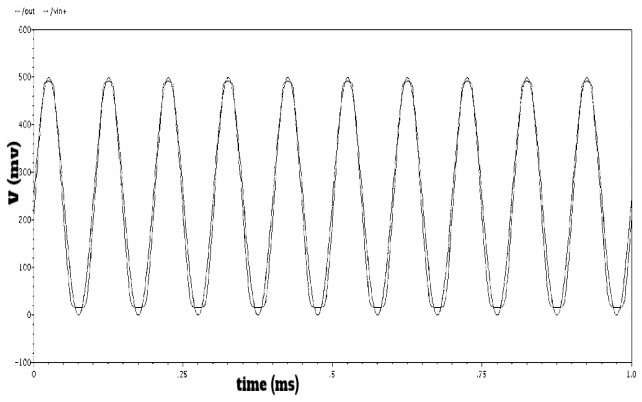


Fig. 9 Rail-to-Rail input and output swing

TABLE I SIMULATED PERFORMANCE OF THE OTA

Parameters	V_{DD} = 0.5 V
DC gain	46 dB
Unity-gain frequency	97 MHz
Phase margin	52˚
Output swing	0.5 V
Slew rate	77.2 V/µs
CMRR	>30 dB
PSRR	>40 dB
Power	124 µW

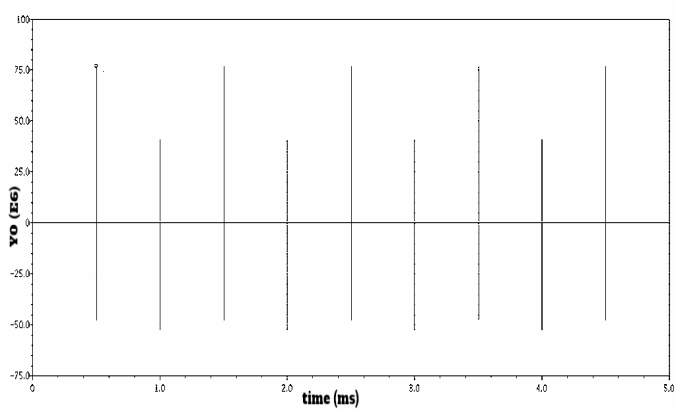


Fig. 10 Slew Rate of Proposed OTA

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