Reduce Leakage Power of SRAM Cell using Variable Body Biasing and Force Sleep Tecnique in Submicron Technology

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***Abstract*— Static power dissipation is an effective field in deep Sub-micron technology. Scaling down of technology and higher operating speeds of CMOS VLSI circuits, the leakage power is increased. As move towards the Sub-micron technology, device consistency and threshold voltage becomes smaller. When reducing the supply voltage result to its reducing the threshold voltage and gate oxide thickness. An increasing in device density and reducing threshold voltage result in higher increases the leakage power. The main determination of the paper work is to reduce the leakage of the SRAM Cell. The circuit of the SRAM Cell is designed using proposed leakage reduction technique(variable voltage biasing technique and force sleep) and compare with previous techniques like sleep transistor, force stack, sleepy stack and simulated in the cadence virtuoso tool using 90nm,180nm technology.**

Keywords- Leakage Power, Gate Oxide, Threshold Voltage, Submicron Technology, Dynamic Power

I. INTRODUCTION

Power consumption is one of the major concerns of VLSI Circuit design, for which CMOS is the primary technology. Today's aim on low power is not only because of the recent increasing demands of mobile applications. Alike before the mobile era, power consumption has been a principal problem. Before the CMOS is scaled down into deep sub process, dynamic power has been dominated, while leakage power is tiny [1]. The assertive scaling of CMOS device achieves higher density, increased performance and lower power consumption. To keep the power consumption under control the supply voltage has been scaled down since the threshold voltage and the transistor has to be scaled to achieve high performance [2].

When threshold voltage scale down sub threshold Leakage Current increases. There are four main sources of leakage in CMOS circuits.

There are four main sources of leakage current in a CMOS transistor [1].

1. Junction leakage
2. Gate induced drain leakage
3. Gate direct-tunneling leakage
4. Sub threshold (Weak Inversion) Leakage

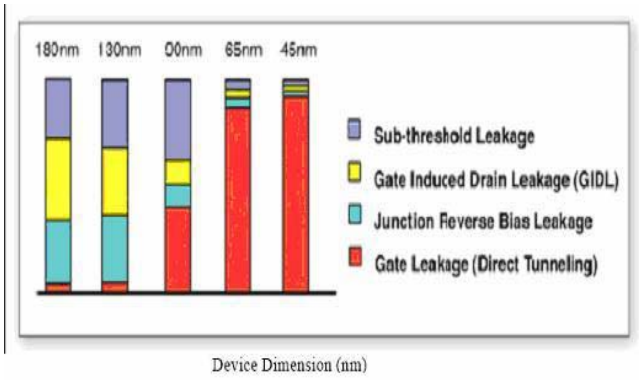

Fig.1. Power Dissipated in various Technology

II. PREVIOUS LEAKAGE REDUCTION TECHNIQUES

Several techniques have been used in the past to reduce leakage power in SRAM cells. Each approach has its own merits and demerits.

A. Sleep Transistor Technique

In this Technique sleep transistors are used at two different position. NMOS sleep transistor is used in the pull down path and PMOS sleep transistor is used in the pull up path of a CMOS circuit. The size of the sleep transistor is obtained with respect to the pull-up or pull-down transistors connected to the sleep transistors. Fig.1 shows the SRAM using the sleep transistor technique. Here the size of the pull-up or pull-down transistors are W/L=6 and W/L=3, so the size of the PMOS and PMOS sleep transistors is W/L=6 and W/L=3 respectively.Sleep transistors are turned on during active mode and turned off during sleep mode. During Active mode the NMOS sleep transistor work at high (logic 1) voltage level and PMOS sleep transistor work at low (logic 0) voltage level.

During standby mode the NMOS sleep transistor is work at low (logic 0) voltage level and PMOS sleep transistor is work at high (logic 1) voltage level.

However, the additional sleep transistors increase delay and area. Furthermore, during sleep mode, the pull-up and pull-down networks will have floating values. The main disadvantage of this technique is that circuit lost exact state in sleep mode operation.

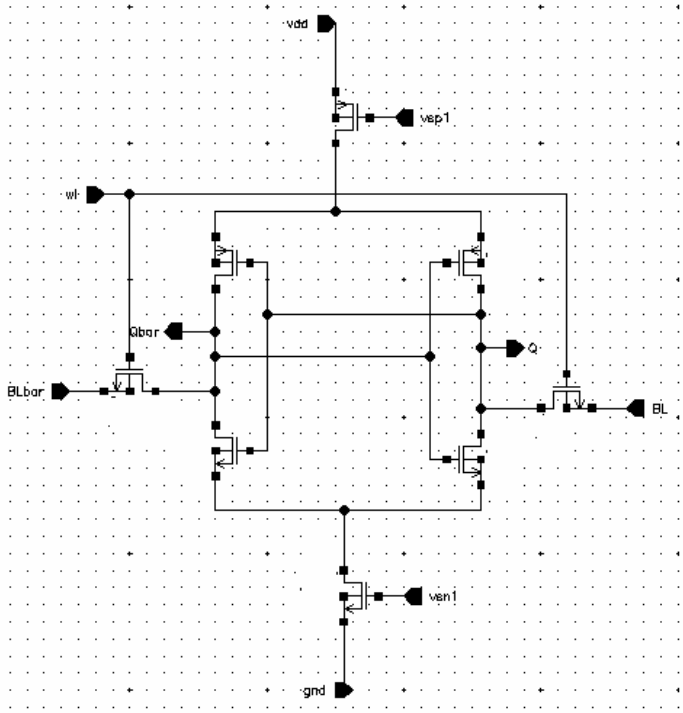

Fig.1. Schematic of Sleep Transistor SRAM Cell

B. FORCE STACK TECHNIQUE

Fig.2 shows the force stack technique, which forces a stack structure by breaking down an existing transistor into two half size transistors. When we apply the force stack technique, we replace each existing transistor with two half sized duplicate transistors. Transistor stacking exploits the stack effect; the stack effect results in substantial sub-threshold leakage current reduction when two or more stacked transistors are turned off together. It obtains considerable current reduction due to the dependence of sub-threshold current on gate bias [8]. By retaining logic state, it overcomes the disadvantage of sleep technique, but main disadvantage of this technique is that it takes more Wake up time. This method uses ratio W/L=1.5 for NMOS transistors and W/L=3 for PMOS transistors.

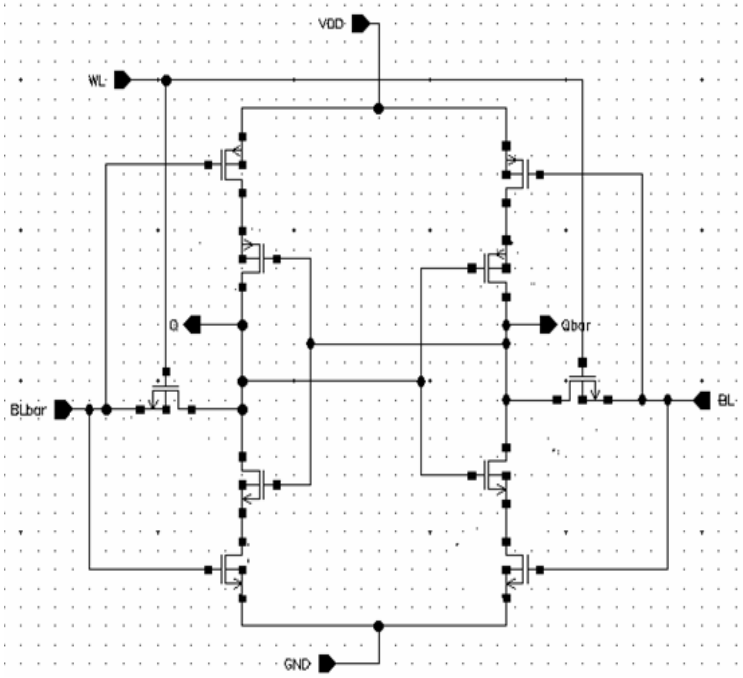

Fig.2: Schematic of Force Stack SRAM Cell

C. SLEEPY STACK TECHNIQUE

Sleepy stack is a novel technique that comprises the existing techniques of sleep transistor and forced stack. This technique cover the advantage of the both. Mainly this technique have lower leakage power dissipation, minimum delay and it's retaining the exact state. In the previous techniques the state may be lost, due to standby mode. The advantages of this technique are to have a state retain, minimal delay and reduced power dissipation. During active mode sleep transistors are in on condition. This sleepy stack structure (in fig.3) reduce circuit delay in two ways. First, since the sleep transistors are always in on condition during active mode, the sleepy stack structure get faster switching time than the force stack structure; specifically, in Fig.3 at each sleep transistor drain, the voltage value connected to the sleep transistor source is always ready and available at the sleep transistor drain, and thus current flow is immediately available to the normal transistors connected to the gate output regardless of the status of each transistor in parallel to sleep transistor.

When the circuit operate in sleep mode all sleep transistors are turned off. When the sleep transistors are turned off, the sleepy stack structure keep exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is reduced by sleep transistors and the transistors parallel to the sleep transistors.

Second, by the reason of stacked effect, which also reduces sub threshold leakage power consumption. By count these two effects, the sleepy stack structure provide ultra-low leakage power consumption during sleep mode while retaining exact logic state. This method uses ratio W/L=1.5 for NMOS transistors and W/L=3 for PMOS transistors within the main SRAM cell portion. For the sleep transistors this technique uses ratio W/L=3 for NMOS and W/L=3 for PMOS transistors[9].

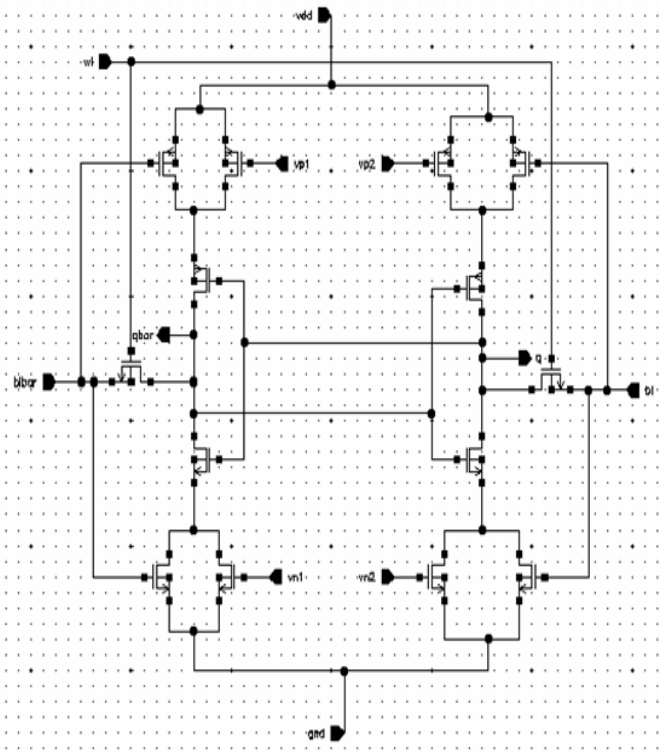

Fig.3. Schematic of Sleep Stack SRAM Cell

III. PROPOSED LEAKAGE REDUCTION TECHNIQUES

A. Variable Body Biasing Technique

This is a new leakage reduction technique, which known as ‘’Variable body biasing’’ technique. This technique (in fig.4) uses two parallel connected sleep transistors in Gnd and two parallel connected sleep transistors in Vdd. The drain of one of the NMOS sleep transistor is coupled to the body of alternative NMOS sleep transistor for having thus known as body biasing effect. Like as the drain of one of the PMOS sleep transistor is coupled to the body of other PMOS sleep transistor for having a related result as for NMOS sleep transistors. So, leakage power is reduced in this technique in two ways. First, due to the sleep transistor effect and second, the body biasing effect. It’s standard that PMOS transistors aren't efficient at passing Gnd; equally, it's standard that NMOS transistors aren't economical at passing Vdd. however this variable body biasing technique uses extra PMOS transistor in Gnd and extra NMOS transistor in Vdd, each area unit in paralleled to the sleep transistors, for maintaining actual logic state throughout sleep mode [10].

This method uses ratio W/L=3 for NMOS transistors and W/L=6 for PMOS transistors within the main SRAM cell portion. In this technique ratio W/L=1 is used for each NMOS and PMOS extra sleep transistors. The additional two transistors of the planning for maintaining the logic state throughout sleep mode conjointly use ratio W/L=1. Attributable to the minimum ratio the sub-threshold leakage current reduces.

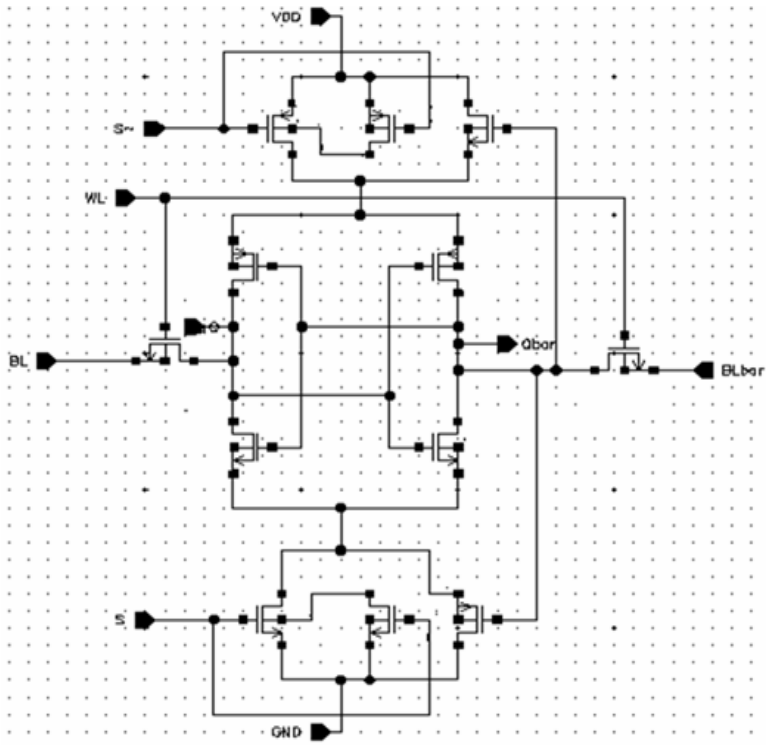

Fig.4 Schematic of Variable Body Biasing SRAM Cell

B. Force Sleep Technique

Force sleep is another new leakage reduction technique. Force sleep technique uses the concept of the force stack technique and the sleep transistor technique. Nevertheless this new method has a delay penalty more than the force stack and sleep transistor technique, this technique is far helpful than any prior approach known to us. The force sleep method can provide ultra-low leakage power consumption. The force sleep SRAM (in Fig.5) uses the ratio of W/L = 3 for the PMOS transistors and W/L = 1.5 for the NMOS transistors. Sleep transistors are further added in series to each set of two stacked transistors in design cell. We use two sleep transistors in circuit, the NMOS sleep transistor with Vdd and the PMOS sleep transistor with ground. Traditionally the NMOS transistor is added to ground because of very capable passing ground voltage and the PMOS transistor is connected to Vdd because it is capable passing Vdd. While in active mode (Fig.5), S = 1 and S’ =0 are stressed, and hence all sleep

transistors are turned on. While in sleep mode (Fig.5), S = 0 and S' =1 are stressed, and that is the reason sleep transistors are turned off.

The leakage reduction in force sleep Structure appear in two ways. First, Leakage power is reduced by the two sleep transistors which are not capable in passing Vdd (NMOS) and ground (PMOS) potential. They will be always in sleep mode at sleep mode operation. Second, two stacked effect and turned off transistors convince the stack effect, which reduces sub threshold leakage during sleep mode. By adding these two effects, the force sleep technique attains ultra-low leakage power consumption while in sleep mode [9].

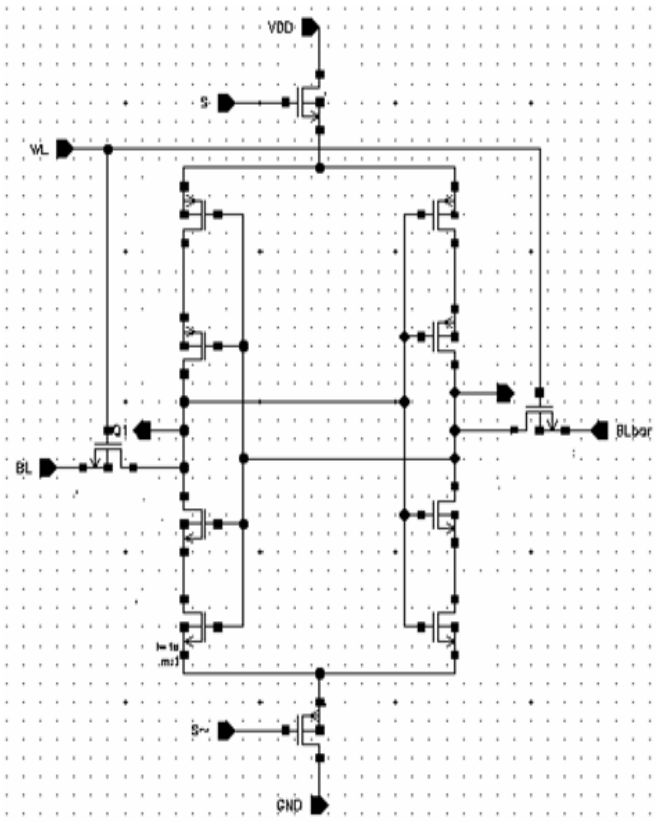

Fig.5. Schematic of Force Sleep SRAM Cell

IV. SIMULATION RESULTS

We compared the variable voltage biasing and force sleep leakage power reduction technique with existing sleepy stack, sleep transistor, force stack transistor technique in terms of power. The results shows that the variable voltage biasing and force sleep technique is producing higher leakage power reduction and it also produces more stability for the circuit. All simulations are performed using 90nm bulk and 180nm bulk MOSFET in cadence tool.

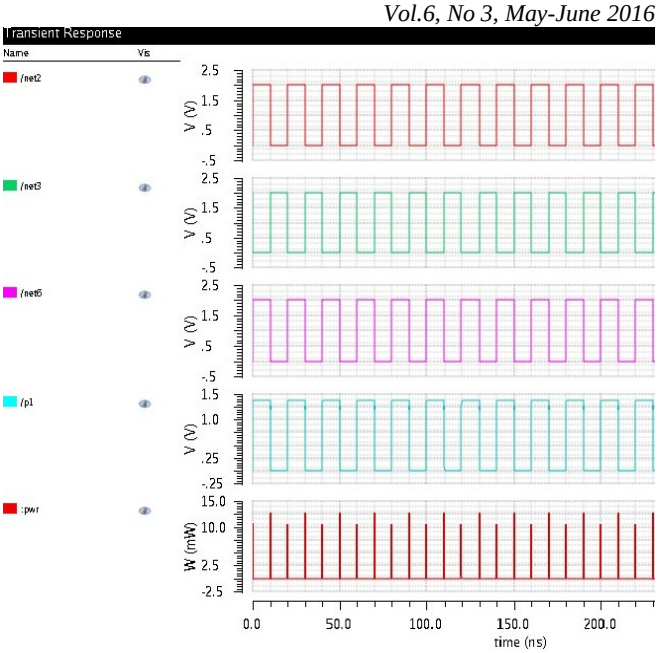

Fig.6. Output of SRAM Cell

Table 1.Static power for various techniques

S.NO.	Techniques	Static power(w) (180nm)@1.8v	Static power(w) (90nm)@1.2v
1.	Sleep transistor	5.42E-05	4.53E-07
2.	Force stack	3.23E-10	3.38E-09
3.	Sleepy stack	5.65E-12	8.46E-11
4.	Variable body biasing	2.46E-13	2.54E-12
5.	Force sleep	1.15E-14	3.28E-13

Table 2.Dynamic power for various techniques

S.NO.	Techniques	Dynamic power(w) (180nm)@1.8v	Dynamic power(w) (90nm)@1.2v
1.	Sleep transistor	6.81E-04	2.71E-04
2.	Forced stack	7.91E-04	3.45E-04
3.	Sleepy stack	9.21E-04	5.91E-04
4.	Variable voltage biasing	5.44E-05	2.36E-05
5.	Force sleep	4.56E-06	1.70E-06

V. CONCLUSION

In sub 90nm technology, the leakage power is high compare to180nm technology.Compared to the all leakage power mechanisms, the sub threshold leakage is dominant proposed new techniques, to efficiently reduce the leakage power named "Variable Body Biasing and Forced Sleep" to overcome the above problem. So variable body bias and force sleep technique achieves ultra low leakage power concumption compare to sleep, force stack and sleepy stack method and maintain the exact logic state in sleep mode.

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